TABLE 1

20 Pin PDIP, SOIC	20 Pin SSOP	Name	Input Type	Pull-up/ Current Source	Output Type	Description
1	1	RA0	ST		N/A	Port Input
		AN0	AN		—	ADC Input
		OPA+	AN		—	Op Amp Non-inverting Input
2	2	RA1	ST		N/A	Port Input
		AN1	AN		—	ADC Input
		OPA-	AN		—	Op amp Inverting Input
7	7	RA2	ST		CMOS	Bi-directional I/O
		AN2	AN		—	ADC Input
		Vref2	AN			Voltage Reference Input for C2 Comparator
8	8	RA3	ST		CMOS	Bi-directional I/O
		AN3	AN		—	ADC Input
		Vref1	AN		—	Voltage Reference Input for C1 Comparator, ADC, and DAC Modules
3	3	RA4	ST		OD	Bi-directional I/O
		T0CKI	ST		—	T0 Clock Input
4	4	RA5	ST		—	Port Input
		MCLR	ST	No	—	Master Clear Input
		Vpp	Power		—	Programming Voltage
17	17	RA6	ST		CMOS	Bi-directional I/O
		OSC2	—		Xtal	Crystal/Resonator
		CLKOUT	—		CMOS	Internal Clock (Fosc/4) Output
18	18	RA7	ST		CMOS	Bi-directional I/O
		OSC1	Xtal		—	Crystal/Resonator
		CLKIN	ST		—	External Clock Input Connection.
		T1CKI	ST			Timer1 External Clock Input

TABLE 1 (cont'd)

20 Pin PDIP, SOIC	20 Pin SSOP	Name	Input Type	Pull-up/ Current Source	Output Type	Description
9	9	RB0	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		INT	ST		—	Interrupt
		AN4	AN		—	ADC, C1, or C2 Comparator Input
		VREF			AN	VREF Reference Output
10	10	RB1	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN5	AN		—	ADC, C1, or C2 Comparator Input
		VDAC			AN	DAC Output
19	19	RB2	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN6	AN		—	ADC, C1, or C2 Comparator Input
20	20	RB3	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN7	AN		—	ADC, C1, or C2 Comparator Input
		OPA			AN	Op Amp Output
11	11	RB4	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
12	12	RB5	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
13	13	RB6	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		PSMC1A			CMOS	PSMC1A Output
		C1			CMOS	C1 Comparator Output
14	14	RB7	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		PSMC1B			CMOS	PSMC1B Output
		C2			CMOS	C2 comparator Output
		T1G	ST		—	Timer1 Gate Input
16	16	Vdd	Power		—	Digital Power
5	5	Vss	Power		—	Digital Ground
15	15	AVdd	Power		—	Analog Power
6	6	AVss	Power		—	Analog Ground

Legend: ST=Schmitt Trigger Input Voltage Levels, CMOS=Complimentary Metal Oxide Semiconductor Output Voltage Levels, TTL=Transistor Transistor Logic Input Voltage Levels, AN=Analog I/O Voltage Levels, OD=Open Drain Output, Xtal=Crystal, RBPU=Port B Pull-Up

TABLE 2A

Alternate Function	PORTA (when not in digital I/O)							
	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
Low Leakage Input only	—	—	—	—	—	—	< 60pA (tested to 50nA)	< 60pA (tested to 50nA)
ADC	—	—	—	—	AN3	AN2	AN1	AN0
Op Amp	—	—	—	—	—	—	OPA- Input	OPA+ Input
VREF Inputs	—	—	—	—	VREF2 Input	VREF1 Input	—	—
Timer0	—	—	—	T0CKI	—	—	—	—
Timer1	T1CKI	—	—	—	—	—	—	—
Oscillator	OSC1/ CLKIN	OSC2/ CLKOUT	—	—	—	—	—	—
Reset	—	—	MCLR	—	—	—	—	—
Programming	—	—	Vpp	—	—	—	—	—

Note 1: Dashed cell implies that the Alternate Function does not apply.

TABLE 2B

Alternate Function	PORTB (when not in digital I/O)							
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
INT	—	—	—	—	—	—	—	INT
ADC	—	—	—	—	AN7	AN6	AN5	AN4
Op amp	—	—	—	—	OPA Output	—	—	—
C2 comparator	C2 Output	—	—	—	AN7	AN6	AN5	AN4
C1 comparator	—	C1 Output	—	—	AN7	AN6	AN5	AN4
VREF Refer-ence	—	—	—	—	—	—	—	VREF Output
DAC	—	—	—	—	—	—	—	VDAC Output
PSMC	PSMC1B Output	PSMC1A Output	—	—	—	—	—	—
Timer1	$\overline{\text{T1G}}$ Input	—	—	—	—	—	—	—
Programming	Data	Clock	—	—	—	—	—	—

Note 1: Dashed cell implies that the Alternate Function does not apply.

TABLE 3

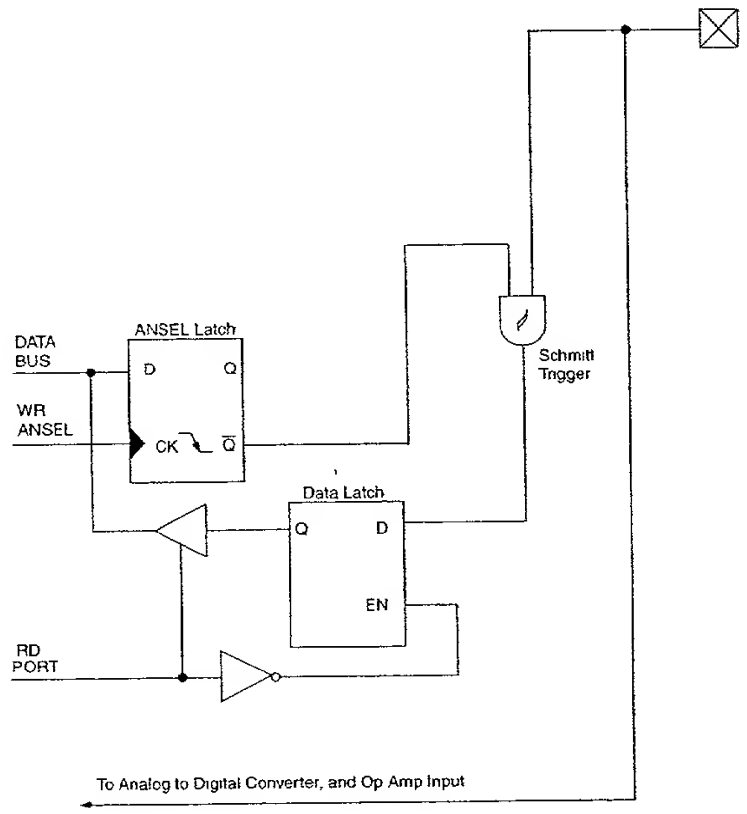
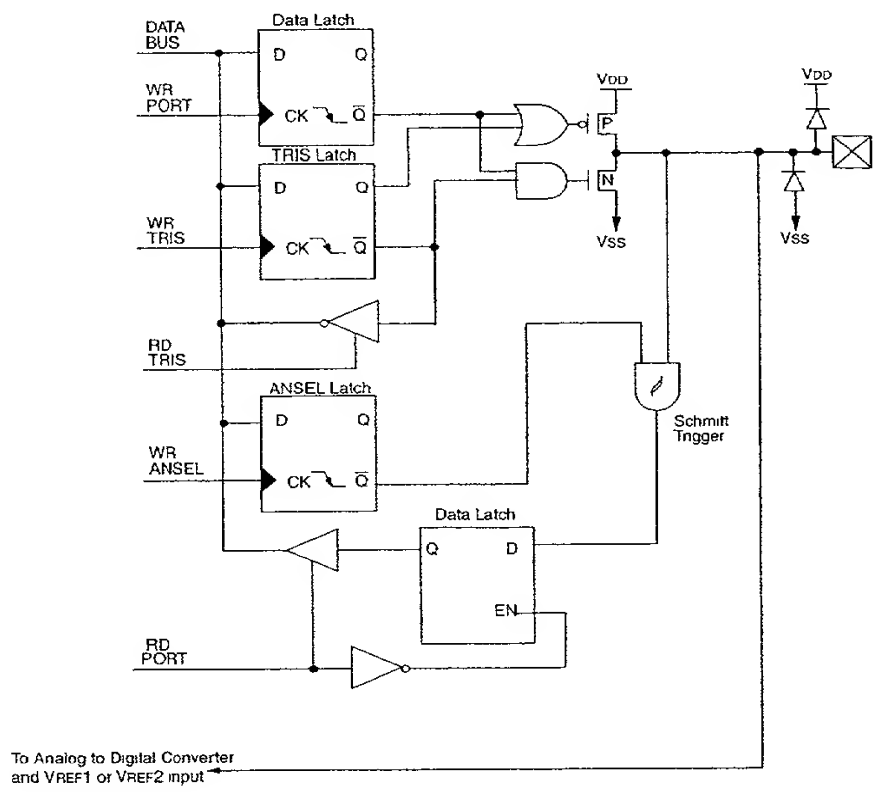
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RA0/AN0/OPA+, RA1/AN1/OPA-	
RA2/AN2/VREF2 AND RA3/AN3/VREF1	

TABLE 3 (cont'd)

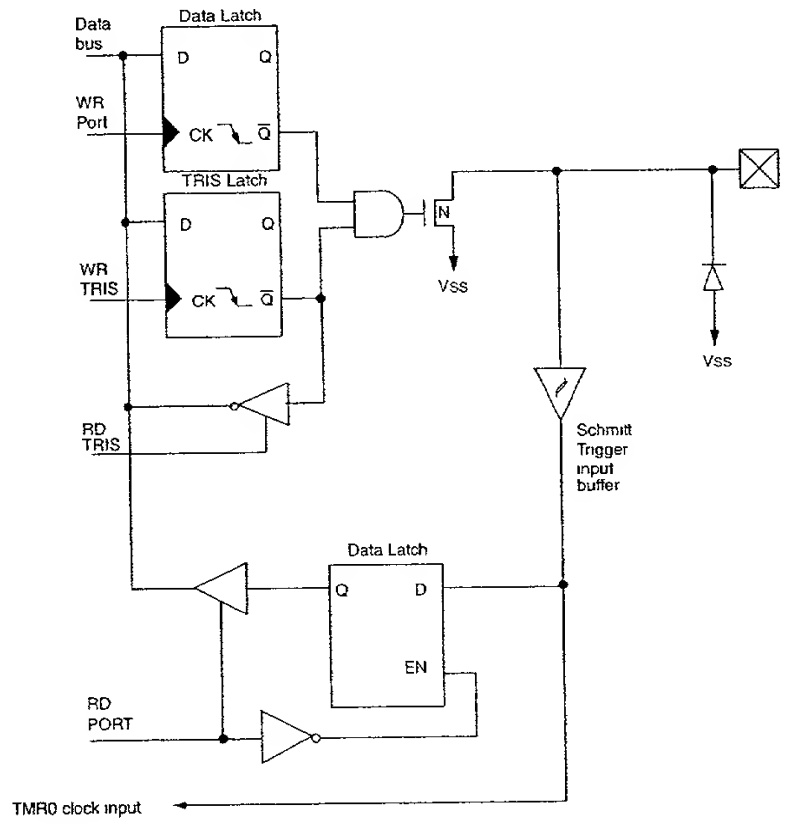
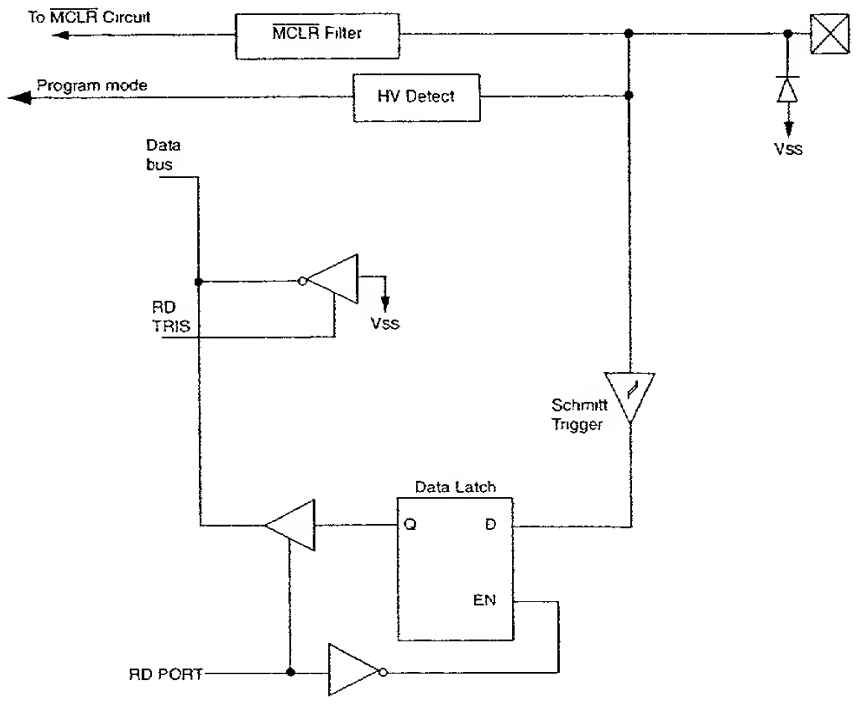
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RA4/T0CKI	
RA5/$\overline{MCLR}$/VPP	

TABLE 3 (cont'd)

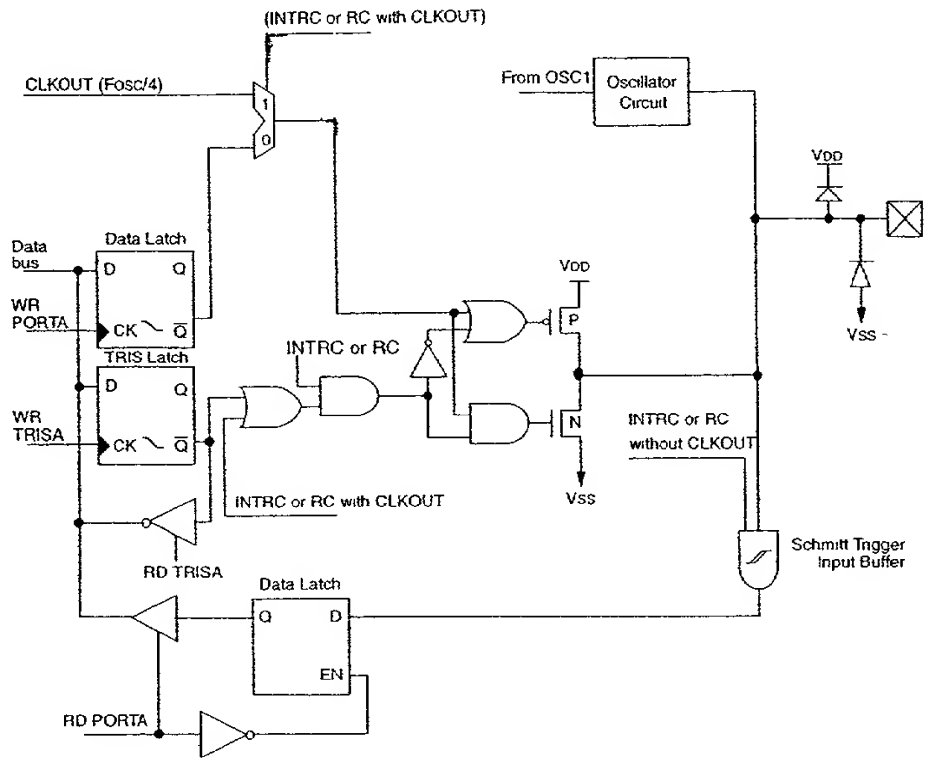
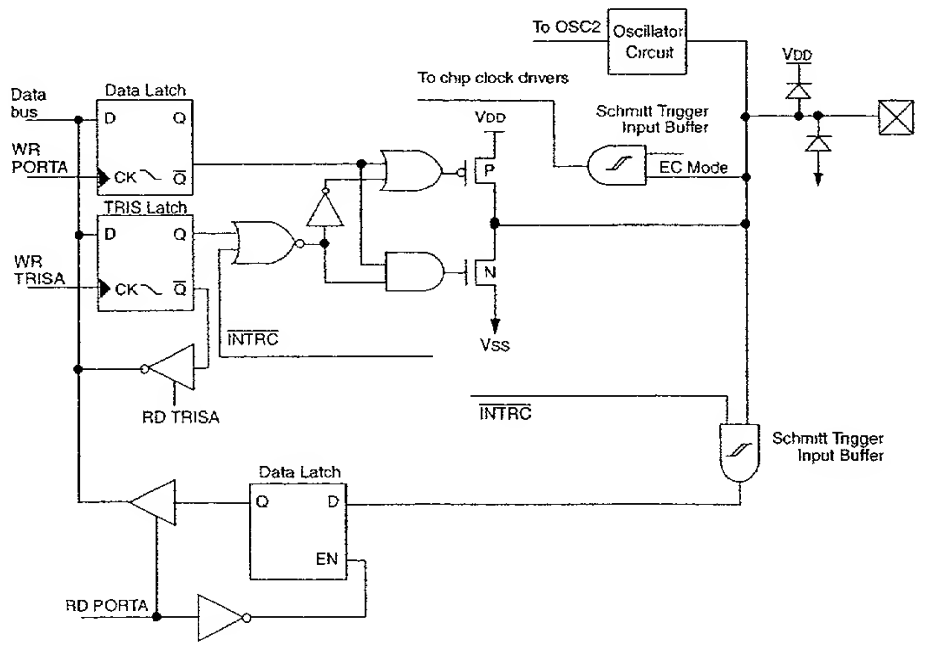
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RA6/OSC2/CLKOUT	
RA7/OSC1/CLKIN	

TABLE 3 (cont'd)

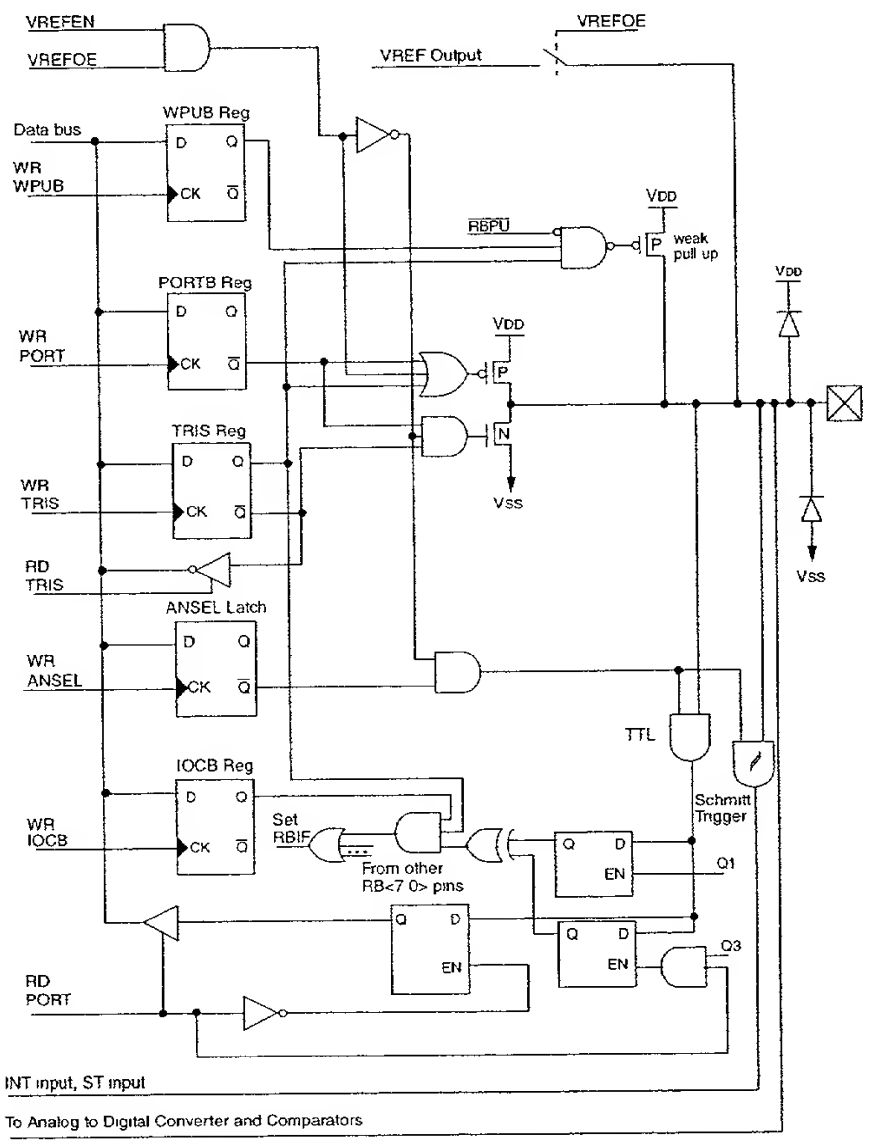
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RB0/INT/AN4/VREF	

TABLE 3 (cont'd)

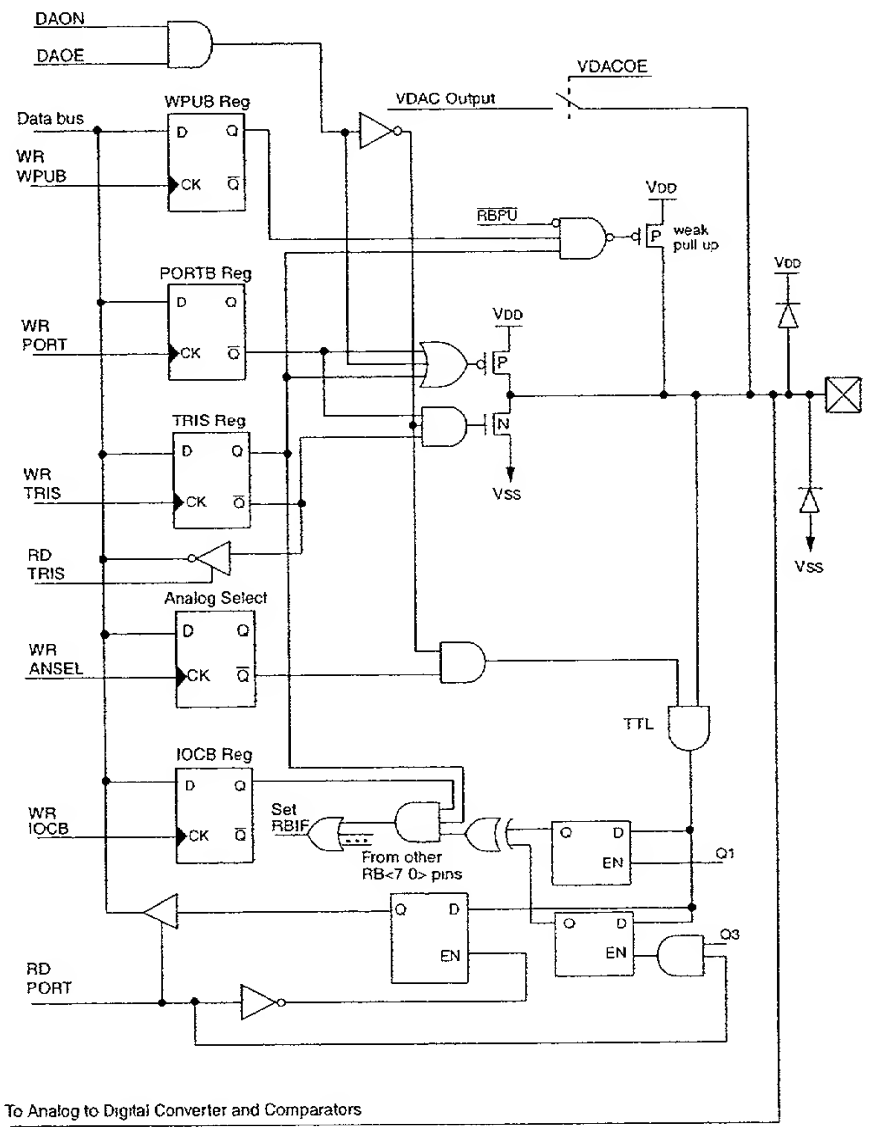
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RB1/AN5/VDAC	

TABLE 3 (cont'd)

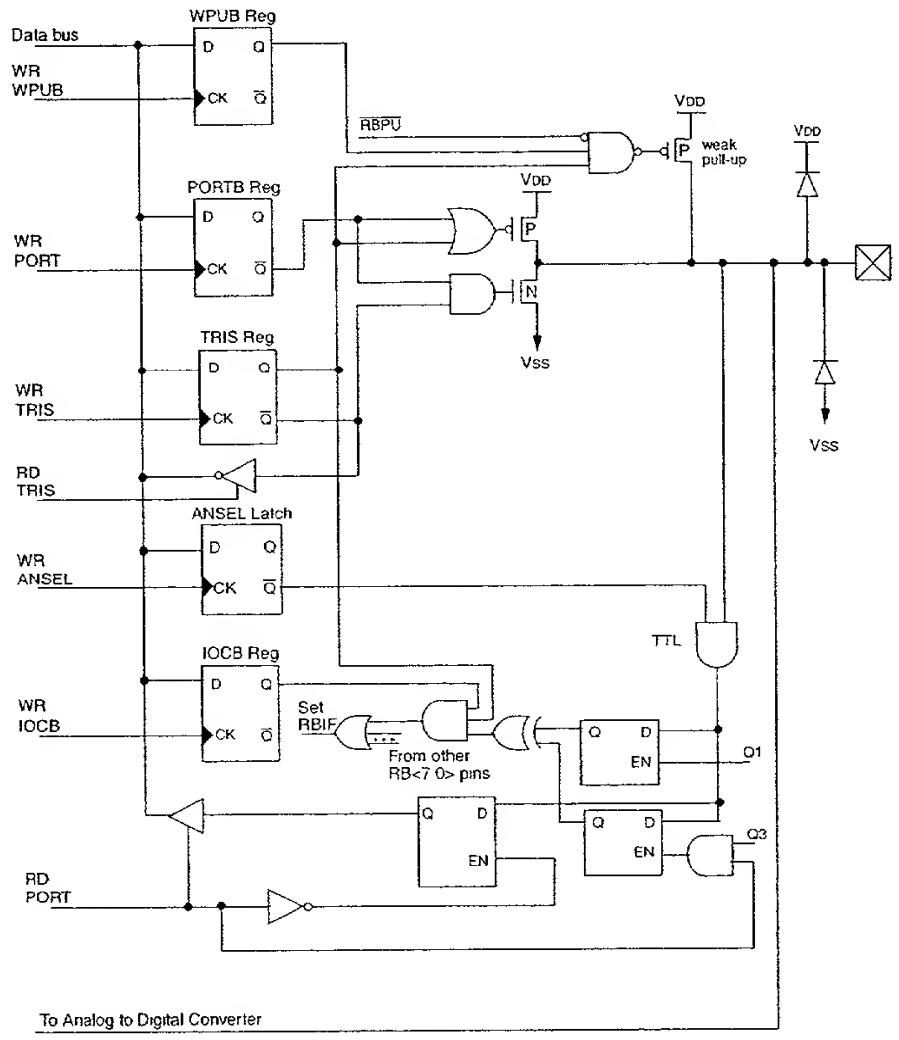
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RB2/AN6	

TABLE 3 (cont'd)

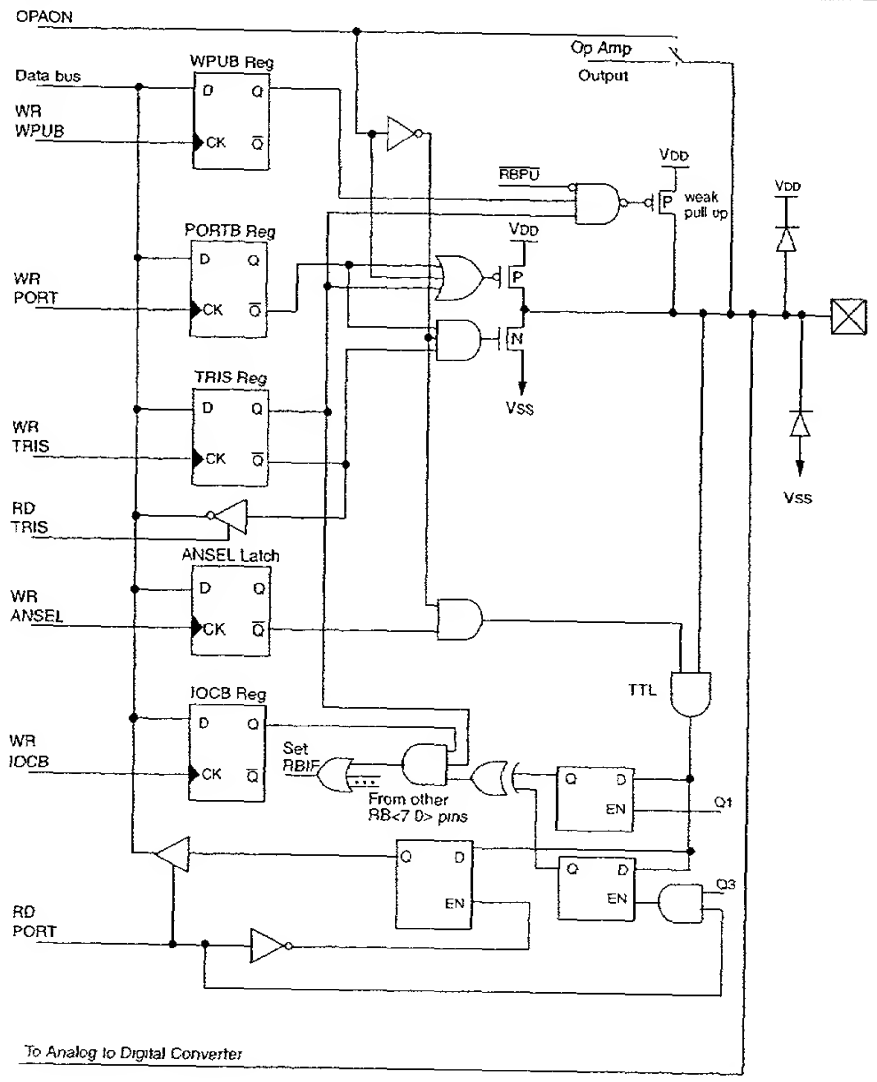
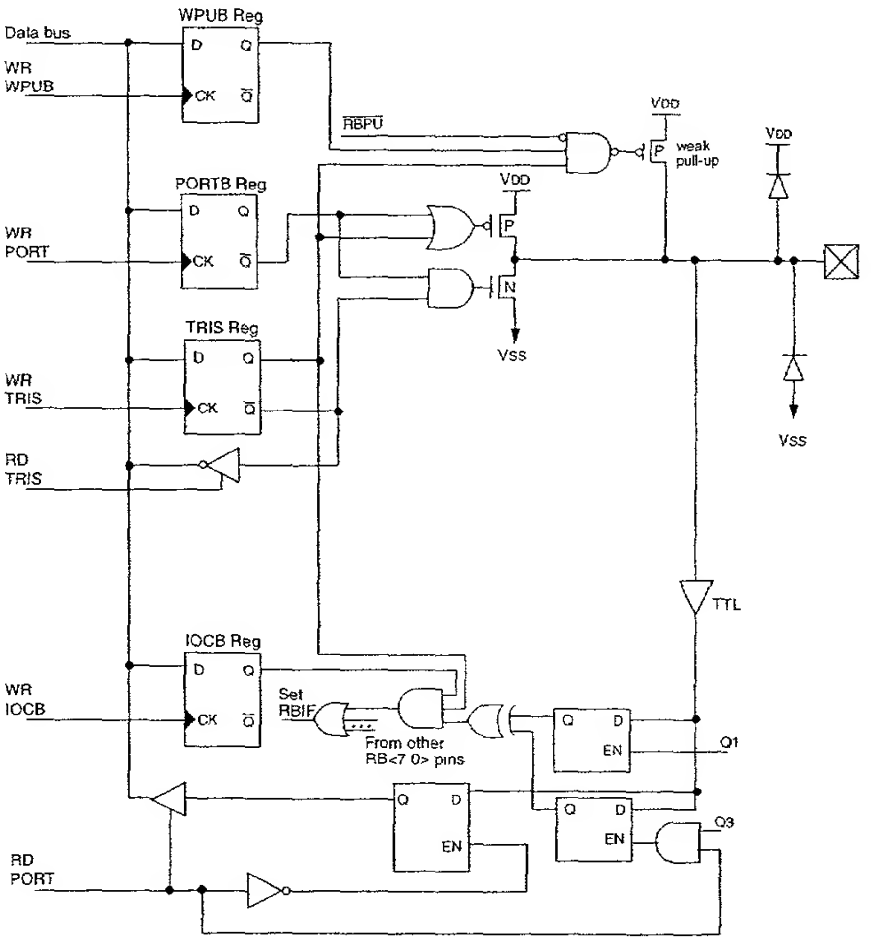
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RB3/AN7/OPA	
RB4 AND RB5	

TABLE 3 (cont'd)

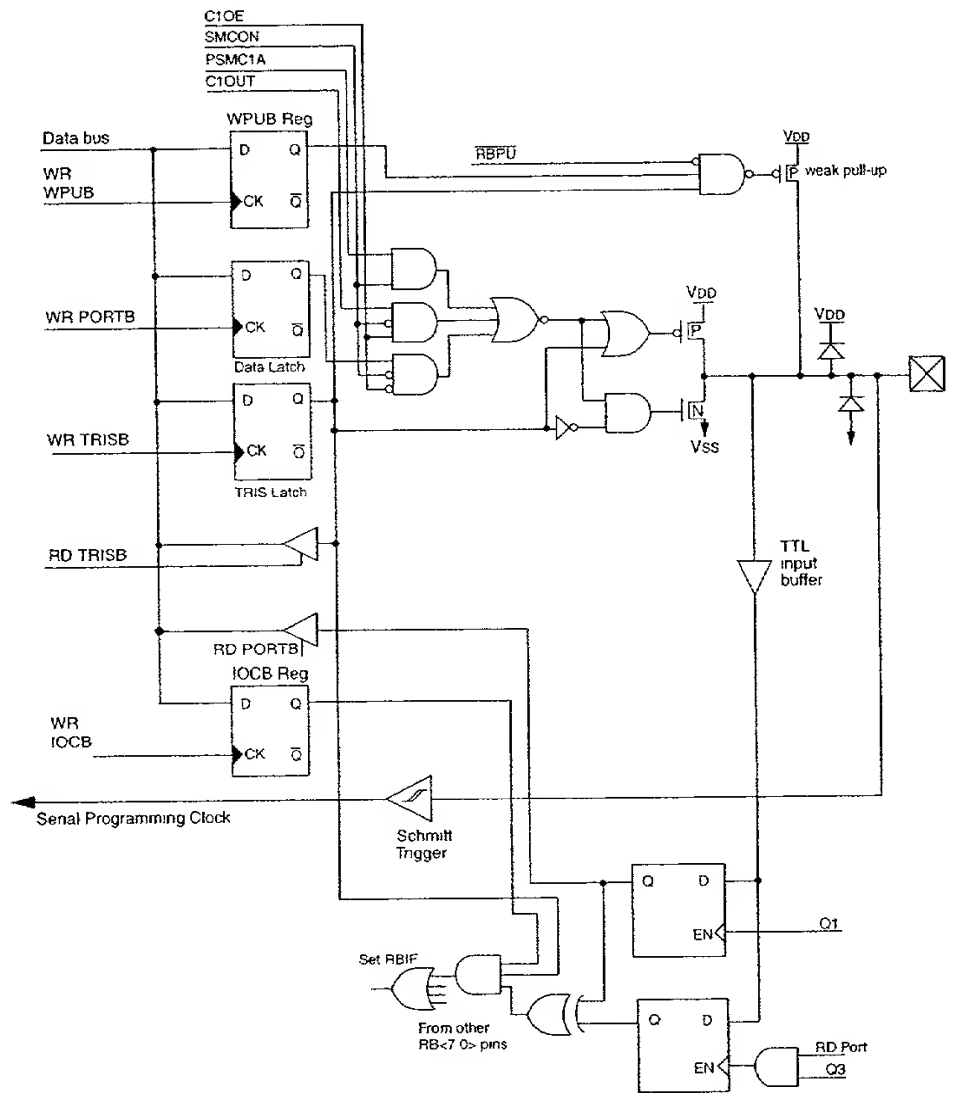
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RB6/C1/PSMC1A	

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RB7/C2/PSMC1B/$\overline{T1G}$